

UNITED STATES PATENT APPLICATION

FOR

**METHODS AND APPARATUS FOR AN IMPROVED DISCRETE
LC FILTER**

Inventor(s)

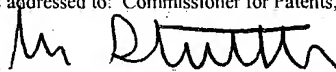
Takatsugu Kamata
Kazunori Okui

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John Stattler

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TITLE OF THE INVENTION

METHODS AND APPARATUS FOR AN IMPROVED DISCRETE LC FILTER

BACKGROUND OF THE INVENTION

Field of the Invention:

5 The present invention is directed toward the field of discrete filters, and more particularly toward capacitor and/or inductor bank filters.

Art Background:

Inductor and capacitor banks may be configured to implement many different types of discrete filters. **Figure 1a** illustrates one embodiment for an inductive (L) bank. For this embodiment, the inductive bank includes five inductors (110, 108, 106, 104 and 102). Although inductive bank 100 includes five inductors, any number of inductors may be used without deviating from the spirit or scope of the invention. The number and values for the inductors is a function of the desired frequency response characteristics of the filter. The inductors, which form inductive bank 100, are configured in parallel. Each inductor is added to the L bank through a corresponding switch as shown in **Figure 1a**. Typically, the switches are implemented using metal oxide semiconductor ("MOS") transistors.

Figure 1b illustrates one embodiment for a capacitive bank. For this example, capacitive bank 120 contains five capacitors (130, 128, 126, 124 and 122). A different number of capacitors and different capacitive values may be selected to implement different frequency responses. Also, as shown in **Figure 1b**, capacitors 128, 126, 124 and 122 are

selected for the C bank through a respective switch. Typically, these switches are implemented with MOS transistors.

Each MOS switching transistor introduces a resistive component into the filter response. Thus, each capacitor selected in the C bank increases the series resistance. The increase in series resistance, or decrease in parallel resistance, decreases the Q factor, which, in turn, degrades performance of the filter bank.

Accordingly, it is desirable to improve the characteristics and performance of an LC filter by reducing parasitic capacitance and increasing the Q factor.

SUMMARY OF THE INVENTION

A discrete inductive-capacitive (LC) filter selects between at least two inductor banks to tune the LC filter for one or more bands of frequencies. The filter receives an input signal for processing. The input signal includes one or more bands of frequencies. A control signal selects a band of frequencies for processing. A first inductor bank, which comprises at least one inductor, is selected to filter a first band of frequencies, and a second inductor bank, which also comprises at least one inductor, is selected to filter a second band of frequencies. A switch circuit couples the input signal to either the first inductor bank or the second inductor bank. The switch circuit selects the first inductor bank if the first band of frequencies is selected, and selects the second inductor bank if the second band of frequencies is selected. The switch circuit electrically isolates the switching of the input signal to the first and the second inductor banks, so as to enhance the Q factor of the LC filter.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1a illustrates one embodiment for an inductive (L) bank.

Figure 1b illustrates one embodiment for a capacitive bank.

Figure 2 is a block diagram illustrating one embodiment for implementing LC filters.

5 **Figure 3** illustrates one embodiment for an input stage of an amplifier.

Figure 4 illustrates one embodiment for an output stage an amplifier that selects between inductor banks.

Figure 5A illustrates one embodiment for electrically coupling capacitors.

10 **Figure 5B** illustrates one embodiment for reducing parasitic capacitance for a capacitor bank.

Figure 6A illustrates an example inductor bank.

Figure 6B illustrates an inductor bank configured in accordance with one embodiment of the present invention.

Figure 7 illustrates a frequency response for an example LC filter.

15 **Figure 8** illustrates an example LC filter.

DETAILED DESCRIPTION

Figure 2 is a block diagram illustrating one embodiment for implementing LC filters.

Circuit 200 includes two signal paths: a signal path for a first band (*e.g.*, Band I), and a signal path for a second band (*e.g.*, Band II, III). In one application, circuit 200 comprises LC filter banks for a television tuner. For the television tuner embodiment, the signal path for “Band I” filters input signals within the frequency range of 50 to 285 MHz, and the signal path for “Band II, II” filters input signals within the frequency range of 285 to 880 MHz.

The signal path for the first band consists of an inductive bank (*i.e.*, transformer) comprising inductors 206 and 208. The inductive bank (inductors 206 and 208) receives the input signal from radio frequency (“RF”) input 202. Circuit 200 further includes, in the first signal path, capacitor bank 220. Capacitor bank 220 comprises a plurality of capacitors selectively coupled to the first signal path. The selective coupling of capacitors in capacitor bank 220 along with inductors 206 and 208 comprise a first tunable LC filter. The output of capacitor bank 220 is input to an amplifier (*e.g.*, automatic gain controlled) 226.

The RF input 202 is also coupled to the second signal path, through capacitor 204, for the second bank of input frequencies (*e.g.*, Bands II, III). The second signal path for the second band consists of an inductor bank, consisting of inductors 210 and 212, and a capacitor bank 222. Capacitor bank 222 comprises a plurality of capacitors selectively coupled to filter the signal in the second signal path. The capacitors of capacitor bank 220 and inductors 210 and 212 comprise a first tunable LC filter for the second signal path. The output of capacitor bank 220 is input to AGC amplifier 226.

The AGC amplifier 226 selectively couples either the first signal path or the second signal path to the output of amplifier 226. For example, in the television tuner embodiment, AGC amplifier 226 selects the first signal path if the television tuner is set to tune a channel in Band I. Alternatively, AGC amplifier 226 selects the second signal path if the television
5 tuner is set to tune a channel in Bands II, III. One embodiment for AGC amplifier 226 is described more fully below in conjunction with a discussion of **Figures 3 and 4**.

For the first signal path, the output of AGC amplifier 226 is coupled to capacitor bank 228. The output of capacitor bank 228 is input to an inductor bank. In turn, the output of the inductor bank is input to capacitor bank 240. For this embodiment, the inductor bank
10 comprises inductors 234 and 236, and tunable capacitors 230 and 232. The capacitors of capacitor banks 228 and 240, similar to capacitor bank 220, are selected to tune the LC filter. The output of the first signal path is input to buffer 254.

For the second signal path, the output of AGC amplifier 226 is coupled to capacitor bank 242. Similar to the first signal path, the output of capacitor bank 242 is input to an
15 inductor bank (*i.e.*, inductors 248, 250 and tunable capacitors 230 and 246). The output of the inductor bank is input to capacitor bank 252. The capacitors of capacitor banks 228 and 240 are selected to tune or program the LC filter. The output of the second signal path is also input to amplifier 254..

The inductors, for the embodiment of **Figure 2**, do not include switches (*e.g.*, MOS
20 transistors), coupled in series with the inductors, for selectively adding inductance to an LC filter. Instead, the input signal (*i.e.*, the signal for processing) is switched in an amplifier

between signal paths (e.g., the first and second signal paths for the embodiment of **Figure 2**).

The elimination of the series resistance in the inductor bank results in a better Q factor for the LC filter. The amplifier, which switches between the first and second signal paths, isolates the resistance from the MOS transistors. Although the embodiment of **Figure 2** isolates the switches in the input and output transistor stages, any configuration to isolate the series resistance of an electronic switch from inductors may be used without deviating from the spirit or scope of the invention.

The LC filter architecture of **Figure 2** minimizes the number of coils. The first and second signal paths are suitable for covering a wide range of input frequencies. For example, in the embodiment of **Figure 2**, only two coils are used for both the first and second signal paths. This architecture has application for use in processing UHF/VHF bands of television signals.

Figures 3 and 4 illustrate one embodiment for input and output stages, respectively, of an amplifier. The amplifier switches between signal paths to effectively select inductor banks for an input signal. In general, the amplifier receives, as input, signals from the first and second signal paths as well as control signals (band and band'). For the first signal path (e.g., signal path for Band I), transistors 328 and 332, when selected, drive the output for this transistor stage. If the second signal path is selected (e.g., signal path for Band II, III), transistors 318 and 320 drive the output for this transistor stage. The differential input signal path includes, for the first signal path, capacitors 326 and 330, and capacitors 318. The second signal path receives a differential signal for input to capacitors 314 and 316.

The control signal, Band, controls the switching of switch 304, for the first signal path, and controls the switching of switches 338 and 340 in the second signal path. The control signal, Band', has a value opposite from the control signal Band. The control signal Band' controls, for the first signal path, the switching of switch 302, and controls the switching of switches 322 and 324 in the second signal path. In one embodiment, the switches (302, 304, 322, 324, 338 and 340) comprise metal oxide semiconductor (MOS) transistors. In operation, to select the first signal path (e.g., Band I), Band is set to a low logic level and Band' is set to a high logic level. Under these control signals, switch 302 is turned on, and switches 338 and 340 are turned off. The activation of switch 302 biases the output transistors (328 and 332) to conduct. As a result, the input signal is conducted through transistors 328 and 332. Also, a low logic level signal on Band turns off switch 304, and a high logic level on Band' turns on switches 322 and 324. When closed, switches 322 and 324 pull the base of transistors 318 and 320 to ground, and the input signal to the second signal path is not passed to the output of the input transistor stage (300).

Conversely, when Band is set to a high logic level and Band' is set to a low logic level, switch 302 is opened and switches 338 and 340 are closed. Under these control signals, the voltage level at the bases of transistors 332 and 328 are pulled to ground, thus turning off transistors 328 and 332. As a result, the input signal from the first signal path is not passed to the output of the input transistor stage (300). Also, a high logic level on Band and a low logic level on Band', closes switch 304 and opens switches 322 and 324. The activation of switch 304 biases the output transistors, 318 and 320, through pull-up of resistors 308 and 306, to conduct. As a result, the input signal to the second signal path is

passed to the output of the input transistor stage (300). Each of the output lines of this transistor stage includes a current buffer, illustrated on **Figure 3** as current sources 334 and 336.

Figure 4 illustrates one embodiment for an output stage an amplifier that selects between inductor banks. The amplifier isolates the switching of transistors and consequently isolates transistor series resistance to the inductor banks. In one embodiment, the output stage of the amplifier comprises a transconductance (g_m) amplifier. For this embodiment, the transconductance amplifier, which converts a voltage to a current, comprises transistors 410, 412, 414, 416, 418 and 420, as well as variable resistors 422 and 426 and current source 428.

To select the first signal path (e.g., Band I), the Band control signal is set to a low logic level, and the Band' control signal is set to a high logic level. A high logic level Band' control signal turns on transistor 404 to place a high logic level at the base of transistors 410 and 412. Consequently, transistors 410 and 420 drive the output for Band I or the first signal path. Also, a high logic level on Band' closes switch 406, pulling the base of transistors 412 and 418 to ground. As a result, transistors 412 and 418 are turned off, and the input does not pass to the second signal path (Band II, III).

Alternatively, to select the second signal path (Bands II, III), the Band control signal is set to a high logic level, and the Band' control signal is set to a low logic level. A high logic level Band' control signal turns on transistor 404 to place a high logic level at the base of transistors 410 and 412. As a result, transistors 412 and 418 drive the output for the second signal path (Band II, III). Also, a low logic level on Band' closes switch 408, pulling

the base of transistors 410 and 420 to ground and turning the transistors off (*i.e.*, the input does not pass to the first signal path (Band I) to the output).

Figure 5A illustrates one embodiment for electrically coupling capacitors. In general, one or more capacitors selectively couple a plurality of capacitors to form a configurable capacitor bank. For the example circuit 500 of **Figure 5A**, capacitors 502 and 506 are coupled through a switch 504. In one embodiment, switch 504 comprises a metal oxide semiconductor (MOS) transistor. A control signal (CT) enables switch 504 so as to electrically connect capacitors 502 and 506.

Figure 5B illustrates one embodiment for reducing parasitic capacitance for a capacitor bank. An example capacitor bank includes capacitors 508 and 512 selectively coupled by MOS transistor (*e.g.*, NMOS) 510. To minimize the parasitic capacitance, the circuit of **Figure 5B** includes transistors 540 and 550. A control signal (CT) is used to select capacitors (508 and 512) to configure a capacitor bank. The control signal (CT) is input to the gates of transistors 540 and 550 as well as the gate of transistor 510 through resistor 520. Transistor 540, when turned on, couples node 560, through resistor 514, to ground. As shown in **Figure 5B**, node 560 is located at a point connecting transistor 510 and capacitor 508. Also, transistor 550 connects, when activated by CT, node 570 to ground through resistor 530. Although the circuit shown in **Figure 5B** may be used to selectively couple two capacitors, the circuit may be duplicated to selectively couple any number of capacitors without deviating from the spirit and scope of the invention.

In operation, to connect capacitors 508 and 512, CT is set to a high logic level. A high logic level on CT turns on transistor 510 to couple capacitors 508 and 512. Also, a high logic level on CT turns transistor 540 on and transistor 550 off. Therefore, transistor 540 lowers the voltage at nodes 560 and 570 by pulling the voltage toward ground through resistors 514 and 530, respectively. In this state (*i.e.*, transistor 510 is turned on), the voltage at nodes 560 and 570 properly bias the transistor. To de-couple capacitors 508 and 512, the CT signal is set to a low logic level. As a result, transistors 540 and 510 are turned off, and transistor 550 is turned on. The activated transistor 550 increases the voltage at nodes 560 and 570 based on resistors 514 and 530 and the bias voltage at transistor 550. Also, a low logic level on CT grounds the voltage at the gate of transistor 510. The increased gate to source voltage of transistor 510, a result of the voltage at the source (*i.e.*, node 570) and the voltage at the gate, reduces the gate-source junction capacitance of transistor 510. Similarly, the increased gate to drain voltage of transistor 510, a result of the voltage at the drain (*i.e.*, node 560) and the voltage at the gate, reduces the drain-source junction capacitance of transistor 510. Thus, the circuit minimizes parasitic capacitance generated from the drain to gate and gate to source junctions on the MOS transistors.

In one embodiment, the filter characteristics of an inductive bank are improved. Specifically, the bandpass characteristic of an inductor bank is improved by tuning capacitance across inductors based on desired characteristics of the filter (*e.g.*, capacitance is selected to adjust a filter based on tuning frequency of a receiver). **Figure 6A** illustrates an example inductor bank. As shown in circuit 600 of **Figure 6A**, inductors 610 and 620 are configured in parallel. The response of the inductor bank 600 is based on, in part, a mutual

coupling factor between inductors 610 and 620. The mutual coupling factor is illustrated in **Figure 6A** by the line with arrows and the symbol, M .

Figure 6B illustrates an inductor bank configured in accordance with one embodiment of the present invention. For this embodiment, the inductor bank comprises inductors 640 and 650. In addition, the inductor bank 630 comprises variable capacitor 660. The variable capacitor 660 is tunable, such that the capacitance introduced may be varied. The variable capacitor 660 may comprise any type of device capable of generating variable capacitance.

In general, the coupling factor for the inductor bank (e.g., transformer) is controlled by introducing capacitance across the inductors (e.g., variable capacitor 660 in circuit 630 of **Figure 6B**). This capacitance is selected based on a tuning frequency of the LC filter. In contrast, the coupling inductor bank 600 of **Figure 6A** is based on the inductors' mutual coupling factor. By selecting a capacitance to tune the coupling factor, a constant bandwidth across variable LC filter characteristics (i.e., center frequencies) may be achieved.

Figure 7 illustrates a frequency response for an example LC filter. For purposes of nomenclature, the bandpass response is characterized by a center frequencies f_c , f_{c1} and f_{c2} . **Figure 8** illustrates an example LC filter. The following terms are used to define various relationships in the LC filter:

BW – Bandwidth

k_c – Capacitive coupling

k_l – Inductive coupling

M = Mutual inductance

The center frequency, f_c , may be defined in accordance with the expression:

$$f_c = \sqrt{f_{c1} * f_{c2}}.$$

The relationship between the frequencies f_{c1} and f_{c2} is based on the bandwidth of the
5 response such that:

$$f_{c1} = BW + f_{c2}.$$

The capacitive coupling factor may be expressed as:

$$k_c = \frac{C_k}{C},$$

and the inductive coupling factor may be expressed as:

10
$$k_l = \frac{M}{L}$$

wherein, "C" and "L" are the capacitances and inductances shown in **Figure 7**. The total
coupling factor may be expressed as a sum of the capacitive and inductive coupling:

$$k = k_c + k_l.$$

The total coupling factor may be expressed as a function of the f_{c1} and f_{c2} frequencies:

15
$$k = \frac{\left(\frac{f_{c1}}{f_{c2}}\right)^2 - 1}{\left(\frac{f_{c1}}{f_{c2}}\right)^2 + 1}$$

Accordingly, the center frequency range (*i.e.*, f_{c1} to f_{c2}) of the bandpass response of the LC filter is tunable based, in part, on the value of the capacitive coupling factor.

Although the present invention has been described in terms of specific exemplary embodiments, it will be appreciated that various modifications and alterations might be made
5 by those skilled in the art without departing from the spirit and scope of the invention.